ADVANCED SUBSTRATE NEWS™
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SOI In Action

The New Generation: It's All On SOI

The PS3, Wii and Xbox 360 CPU design teams all chose SOI. Here's why.

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(Courtesy: Sony Computer Entertainment Europe)

PlayStation®3 "Cell" CPU. Jointly developed by IBM, Sony and Toshiba. Manufactured by IBM and Sony. (Courtesy: IBM)

Design challenges: Achieve 100 times the PlayStation®2 performance. Joint developers IBM, Sony Group and Toshiba needed to co-optimize the chip area, design frequency, and product operating voltage, creating a "supercomputer on a chip" that marries broadband interconnect, entertainment systems, and supercomputer structures. Beyond the PlayStation®3, the three companies would each promote Cell-based products ranging from digital televisions to home servers to supercomputers.

Solution: Multi-core SoC architecture featuring eight synergistic processors (PowerPC-base Core @3.2GHz, 8 x SPE @3.2GHz). 234 million transistors. 90nm SOI CMOS.

Result: SOI provides a significant power/performance advantage.

(Courtesy: Nintendo)

Design challenges: Wii console to be no bigger than a stack of three DVD cases so it fits inconspicuously next to a TV and can be left on 24 hours a day. Need lower power consumption and higher performance in a smaller chip. Small case incurs severe heat restrictions.

Solution: Custom PowerPC (code-named "Broadway") on 90nm SOI CMOS.

Result: SOI technology from IBM helps deliver to Nintendo a generous improvement in processing power while achieving a 20 percent reduction in energy consumption.

Wii™ CPU. Jointly developed by Nintendo and IBM. Manufactured by IBM. (Courtesy: IBM)

(Courtesy: Microsoft)

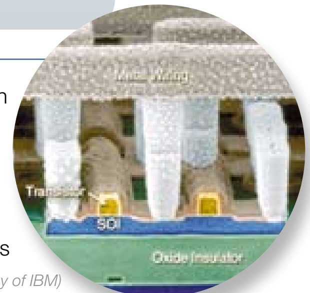
Xbox™360 CPU. Jointly developed by Microsoft and IBM. Manufactured by IBM and Chartered. (Courtesy: IBM DeveloperWorks)

Design challenges: Ground-up design specifically for high-definition gaming and entertainment. Chip design from concept to full execution in 24 months. Pack twice the power of the Xbox into a smaller form factor. Give game designers power where they need it.

Solution: A customized version of IBM's 64-bit PowerPC core. The chip includes three of these cores, each with two simultaneous threads and clock speeds greater than 3.2 GHz. 165 million transistors. 90nm SOI CMOS, transitioning to 65nm SOI in Q107.

Result: SOI technology reduces heat and improves performance.

"The CPUs for the leading, next-generation game consoles are built on IBM's SOI CMOS technology. In each case, the design teams had specific goals regarding how they wanted to manage their power budgets. SOI provides a key tool in balancing their requirements in terms of performance, power consumption, chip size, heat and cost." — Ron Martino, Director, IBM Technology Collaboration Solutions



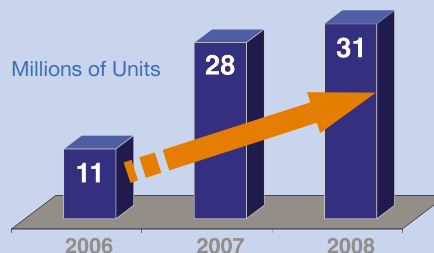
SEM image of SOI transistors. (Courtesy of IBM)

Market Place

"The next three years should see a rapid emergence of the new, high-end game systems from Sony, Microsoft and Nintendo. These systems will quickly replace the current generation of game hardware that has sold over 150 million units since it was introduced in the 2000/2001 timeframe."

David Cole
President, DFC Intelligence

Games Console Forecast
for the PS3 / Wii / Xbox 360 (combined)



Source: DFC Intelligence (November 2006)

END-USER APP

Hitachi's tiny µ-chip

Already the world's smallest RFID chip, SOI makes the next generation far thinner than a piece of paper – while radically increasing productivity.

The next generation of Hitachi's µ-chip (mu-chip) is poised to make a major impact on the RFID (radio frequency identification) world. Presented at the IEEE conference in February 2006, this latest version of the world's smallest RFID chip is based on SOI technology. The result is a chip so small, so thin, that it easily leaves the others behind by at least two generations.

How small is small? Consider it this way. The µ-chip that has been in mass production since 2001 measures 0.4mm on a side – so you could hide it comfortably under a grain of salt. The newest generation µ-chip on SOI measures 0.15mm on a side – so you could hide about a dozen of them under that same grain of salt.

How thin is thin? The current generation is 60 microns thick – about three-quarters as thick as a piece of paper, which is typically about 80 microns thick. The new generation on SOI is only 7.5 microns thick – so a stack of 10 would still be less thick than a piece of paper.

For Hitachi, these SOI-enabled smaller dimensions translate into two very important advantages:

1. **Substantially lower cost of ownership.** With SOI, each device is surrounded by insulator, preventing interference between devices and enabling higher integration on an even smaller area. With the smaller chips, more fit on a wafer – in this case as much as seven times as many. That makes for dramatically lower manufacturing costs – which could potentially enable the company to break the 5-cent barrier that analysts say is needed to really launch the RFID revolution.
2. **The ability to embed the chips in paper.** This opens the door to a whole new realm of applications. Anywhere paper and security considerations intersect, the new µ-chip is a very attractive contender. The extreme thinness was achieved by completely removing the supporting silicon layer, leaving only the top silicon layer in which the circuit is fabricated, and the layer of insulation beneath it.

Now that they're on SOI, you could hide a dozen µ-chips under a grain of salt, and a stack of 10 would still be less thick than a regular sheet of paper.

Thanks to SOI, the newest generation of Hitachi's µ is the world's smallest RFID chip – far smaller than even these grains of salt. (Courtesy: Hitachi)

To help fight counterfeiting and improve supply-chain management, Winwatch of Switzerland has IP for embedding RFID chips such as the µ into the glass, hands or axis of high-end watches. (Courtesy of Winwatch)

Lowering costs

Until now, cost has been a major impediment to large-scale RFID deployment. The current generation µ-chip plus antenna was selling in the 10- to 15-cent range. With the massive increase in productivity enabled by the smaller chip, Hitachi should be well positioned to bring prices down further.

Says Sarah LoPrinzi, BCC Research Analyst and author of "RFID: Technology, Applications and Market Potential" (August 2006), "Hitachi's recent announcement of the next generation of µ-chips resolves some of the technical and economic chip manufacturing issues that have impeded the development of low cost RFID tags. In the RFID industry, the magical cost-per-tag is widely thought to be \$0.05/tag. Once the \$0.05 barrier is overcome, item-level inventory control becomes more realistic."

Moving the µ to SOI, Hitachi has witnessed a 10-fold increase in productivity over the currently deployed bulk chip.

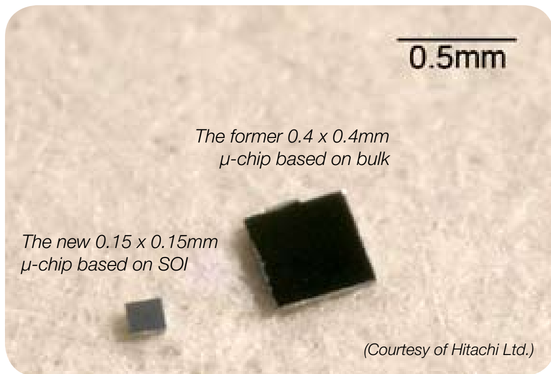
Put it in the paper

The new, ultra-thin µ-chip opens the doors to a wider range of paper-based applications, acting as an "intelligent watermark".

As Mark Roberti, editor-in-chief of the *RFID Journal*, told ASN, "The value in having an ultra-thin RFID tag is that companies can embed the tag in packaging materials for product authentication and anti-counterfeiting applications without worrying that the transponder will be so visible as to make the packaging unattractive." Retail gift

With appropriate packaging, the µ-chip can be attached to a metal object without concern for interference; plus, it can withstand hot and dirty conditions. In Japan, it is used extensively for supply-chain management in industries such as steel.

Photo Credit : Luis Veiga / Getty Images



certificates, labels and other paper documents would benefit from enhanced security.

An obvious application might seem to be banknotes, but this is probably not for the very near-term. While embedding the newest ultra-thin μ-chip in paper currency is now entirely feasible from a technical standpoint, there still remain issues for government and public debate regarding privacy and security in the supporting infrastructure design.

But with both businesses and governments looking for more reliable, cost-effective electronic solutions for managing supply chains and preventing fraud, the tiny μ-chip should be a major player.

The μ-chip is being used for animal tagging in East Asia to ensure traceability in the food supply chain. (Courtesy of Hitachi America)

The new μ

Dimensions
0.15mm x 0.15mm, 7.5 microns thick

Process technology
180nm SOI CMOS (will transition to smaller geometries with volume ramp)

Power
Passive (no battery)

Data storage
128-bit read-only, capable of holding one of 10^{38} unique identity codes.

Frequency
2.45 GHz frequency (same as Bluetooth), so with appropriate packaging it can be attached to a metal object without concern for interference.

Read distance
Close range (30cm with external antenna)

Concept
The chip can only store data encoded during its fabrication (unique ID number plus optional info such as company name, program, denomination, etc.). It cannot record or emit personal data. To emit its ID information, the device uses the microwave sent by the “reader” to generate electric power, decode its ID data and transmit the data back to the reader (response time: 20ms).

Packaging
Double-surface electrode for easy connection with external antenna. Wire bonding or tape carrier package (TCP).

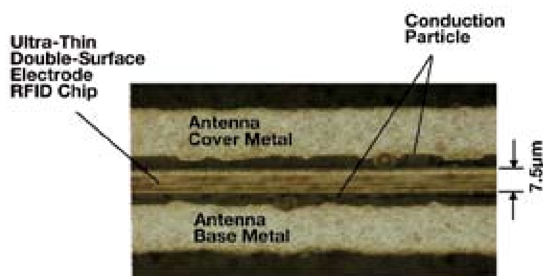
Applications
Security, transportation, amusement, traceability and logistics – any place that barcoding is either impractical or not sufficiently secure. Particularly suited as an “intelligent watermark” for embedding in paper.

Availability
2007

Full use of SOI advantages enables small, thin, and low-cost RFIDs

A lead developer of Hitachi’s μ-chip explains the SOI benefits.

By Dr. Mitsuo Usami, Senior Chief Researcher, Hitachi, Ltd., www.hitachi.co.jp



A cross-sectional view of the ultra-thin μ-chip is shown in the figure, where the chip is sandwiched in the antenna by using ACF (anisotropic conductive film). (Courtesy: Hitachi, Ltd.)

By using SOI, we could make an ultra-small RFID chip. In particular, its excellent isolation capability enabled successful miniaturization of the analog circuits in the front-end of the part. Also, BOX (Buried OXide) acts as an etch-stop layer in the self-controlled process, resulting in an ultimately-thin chip, which is as thin as 7.5 microns (including the multi-layered interconnection). A cross-sectional view of the ultra-thin chip is shown in the figure, where the chip is sandwiched in the antenna by using ACF (anisotropic conductive film). All of these contribute to the realization of low-cost, reliable, and widely-applicable RFIDs.

ON THE CIRCUIT

Thin BOX: A Solution for High-Speed, Low-Power SoCs

By Dr. Ryuta Tsuchiya, ULSI Research Department, Central Research Laboratory, Hitachi Ltd., www.hitachi.com

Control of Si substrate bias in "Silicon on Thin BOX" suppresses leakage current at 45nm and beyond.

Leakage currents in MOSFETs, originating in scattering from device features, pose a serious challenge in high-performance, low-power SoCs (system-on-a-chip), which are applicable to mobile products. The situation becomes more critical at the 45nm technology node.

Hitachi and Renesas are developing a novel structure, "Silicon on Thin BOX", where the buried oxide (BOX) is approximately 10nm thick, enabling the control of MOSFET characteristics by biasing the Si substrate [Ref]. "Silicon on Thin BOX" is expected to provide a solution for simultaneously achieving high-speed and low-power at the 45nm technology node and beyond.

Si substrate as back gate

Figure 1 shows the "Silicon on Thin BOX" structure, with a BOX film of 10nm. As a result, the Si substrate (the "handle" or "mechanical support" of the SOI wafer) can be used as the second gate (back gate), achieving a 20% increase in the operation current. Stand-by leakage is reduced by over 90% -- more than one order of magnitude.

Stand-by leakage is reduced by over 90% -- more than one order of magnitude.

In the actual structure, multiple threshold voltages becomes available, by work-function control through the fully-silicided metal gate structure (FUSI) using NiSi, as well as impurity-doping underneath a BOX layer, as shown in Figure 2. Moreover, unlike bulk Si devices, there is no need for doping in the channel region to suppress the short channel effect. This eliminates the scattering of threshold voltage caused by the statistical fluctuation of impurity atoms, which is known to become a dominant mechanism in a short channel region. This is expected to contribute to the lowering of the minimum operation voltage, enabling further power reduction.

[Ref.] R. Tsuchiya, M. Horiuchi, S. Kimura, M. Yamaoka, T. Kawahara, S. Maegawa, T. Ipposhi, Y. Ohji, and H. Matsuoka, "Silicon on Thin BOX: A New Paradigm of The CMOSFET for Low-Power and High-Performance Application Featuring Wide-Range Back-Bias Control," IEDM 2004 Tech. Dig., pp. 631-634, (2004).

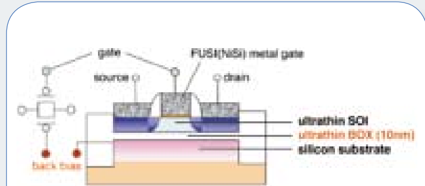


Figure 1. A schematic cross-sectional view of "Silicon on Thin BOX". By reducing the BOX layer to 10nm, the Si substrate can be used as the second gate (back gate).

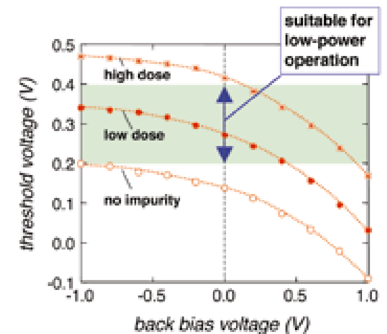


Figure 2. Threshold voltage (V_{th}) control in a "Silicon on Thin BOX" structure. Multiple threshold voltages becomes possible through the work-function of the NiSi gate electrode, as well as impurity doping underneath the BOX layer by varying the doping level.

Floating Body RAM Becomes an Industrial Reality

By Dr. Takeshi Hamamoto, Chief Scientist, Center for Semiconductor Research & Development, Semiconductor Company, Toshiba Corporation, www.toshiba.com

Toshiba has successfully developed a high-performance, high-density, low-cost 128Mb FBRAM.

FBRAM is Random Access Memory (RAM) with a Floating Body Cell (FBC). It is a capacitor-less DRAM cell consisting of a MOSFET on an SOI wafer. Data "1" and Data "0" are distinguished by the hole density in the floating body of the MOSFET.

The conventional DRAM cell consists of a capacitor and a transistor, whereas an FBC, consisting of only a transistor, provides three kinds of advantages:

- **Scalability:** there is no need for 3-dimensional capacitor structures (like a stack and a trench capacitor, which are both approaching the "red brick wall").
- **High performance:** there is no parasitic resistance (as with a poly-Si plug in a stack capacitor).
- **Low cost:** unlike a stack or trench capacitor, there are no additional processes. FBC can be fabricated alongside conventional logic devices.

Fabrication on UT-BOX SOI

To verify the FBC technology, a 128Mb FBRAM has been designed and fabricated based on 90nm-SOI technology. Figure 1 shows a cross-sectional picture of the memory cell-array along the Bit Line (BL) direction. The thicknesses of silicon and buried oxide are 55nm and 25nm, respectively.

An ultra thin BOX has been used in order to stabilize the body potential, which has led to enhancement of the storage signal. The gate electrode of a MOSFET is used as a Word Line (WL). Two layers of copper wiring are used. The 1st Cu wiring is used as a Source Line (SL), which is connected to the source of MOSFET. The 2nd Cu wiring is used as a Bit Line (BL), which is connected to the drain of MOSFET.

FBC is a promising embedded memory structure for SoC on SOI.

The features of the fabricated 128Mb FBRAM device shown in Figure 2 are as follows:

- Design Rule : 90nm-node technology.
- Power supply : 3.3V.
- Chip size : 64.6 mm² (7.6 mm × 8.5 mm).
- Random Access : 18.5 nsec.
- Random Cycle : 25 nsec (read), 32 nsec (write).
- Cell size : 0.17 μm² (0.33 μm × 0.515 μm).
- Wiring : Cu 6 layers.

A 128Mb FBRAM with FBC has been successfully fabricated. We have already obtained good die, good yield, and good retention characteristics. FBC is a promising embedded memory structure for system-on-a-chip (SoC) on SOI.

Fig.1 TEM cross-section along Bit-line

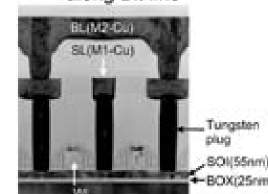


Fig.2 128Mb FBRAM chip

Embedded Memories in SOI

By Subramanian S. Iyer, Distinguished Engineer & Director, 45nm and eTechnology Development,
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www.ibm.com

Embedded DRAM on SOI is set to proliferate at the 45nm node.

Embedded memory now occupies close to 75% of the total chip area. Until a few years ago, this memory was exclusively SRAM, but more recently the industry has seen a significant transition to embedded DRAMs (eDRAMs).

There are several driving forces for this transition:

- Larger caches that are electrically closer to high-speed, multi-core processors. A DRAM cell is 5-8 times smaller than an SRAM cell. At the functional level, DRAMs occupy 3-4 times less area per MB than SRAMs.
- Power – DRAMs tend to have leakage currents about 1000x lower than SRAMs on a per cell basis.
- Soft error rates, which are thousands of times lower in DRAMs.
- Greater cell stability for DRAMs, especially at lower voltages.

However, DRAMs add a bit more complexity than SRAMs to a logic chip, and the fastest DRAMs tend to be slower by a factor of 2-3. Therefore a typical processor IC will use a judicious combination of SRAM for the smaller-size, lower-level caches (where speed is important) and DRAMs for the larger-size, higher-level caches (where density is crucial).

> The complexity adder is about half in SOI compared to bulk for deep trench based eDRAMs.

The case for SOI

To date all eDRAM applications have been in bulk CMOS technology.

But as advanced processors migrate to SOI, there is a need to adapt eDRAM to SOI.

It is relatively straightforward to build a conventional DRAM cell in SOI and in fact for deep trench cells it is simpler. The complexity adder is about half in SOI compared to bulk for deep trench based eDRAMs as shown in Figure 1, where the buried oxide is used to completely isolate the capacitor plate from the device. (A stacked capacitor DRAM can also be fabricated in SOI though there is no cost advantage going to SOI.)

Figure 1. A cross section of a 45nm SOI trench cell.

The migration of established DRAM technologies that have been proven over several generations in bulk promises to be the quickest and least risky way to embed DRAMs in SOI logic.

In addition, there are several novel ideas that leverage SOI-specific effects such as the floating body and back gate interface. These offer the prospect of further simplification if they can be proven in production. We expect the use of eDRAM to proliferate to SOI in the 45nm generation.

Harnessing SOI's Floating Body Effect for Dense Memory Cells

By Pierre Fazan, Chairman & CTO, Innovative Silicon,
www.innovativesilicon.com

The co-inventor of Z-RAM explains the technology.

As a Z-RAM – zero capacitor RAM – memory technology bit cell uses only a transistor plus the floating body effect inherent in SOI processing (see Figure 1), it typically measures only 15-20F^2 (where F is the technology minimum feature size).

Compared with SRAM (where the six transistor bit cell measures around 150 F^2), or embedded DRAM (which requires a capacitor for a bit cell size of 30-40F^2), the density advantages of Z-RAM are obvious.

When Z-RAM replaces eDRAM, silicon estate is halved; when used to replace SRAM, the space savings are 80%. It uses standard SOI logic processes without new materials, extra process or masking steps. The savings can be leveraged to either massively reduce cost or to include more functions on the chip.

Speed, Power or Density

The key drivers for electronic circuitry are density, speed and power. As Figure 2 shows, Z-RAM can be optimized for any of these three parameters.

As speed is dependent mainly on the capacitance of the bit line, for fast access times the bit line can be shortened to deliver up to 400MHz array speed at 65nm. For low power operation, although a shorter bit line does reduce power the effect is not that great since the change in bit line voltage is small. However, by reducing the Word Line length and hence the Word Line capacitance, active power levels of only 10Wμ/MHz at 65nm are achievable.

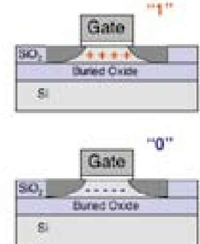
> ISi signed its first license with AMD earlier this year, which will allow the microprocessor company to use Z-RAM memories in next-generation processors.

To achieve the ultimate in array density (>5Mbit/mm^2), longer Word Lines and Bit Lines are required. However this is obviously at the expense of access time and power.

Z-RAM memory technology was co-invented by Pierre Fazan and Serguei Okhonin, who also co-founded Innovative Silicon Inc. (ISi) to commercialize the technology.

Figure 1. Innovative Silicon's Z-RAM™ Technology

In a Z-RAM bit cell, the Floating Body is used as a storage node. An accumulation of holes in the Floating Body defines a first memory state, while the emission of holes by junction forward biasing defines a second memory state. The current through the transistor during a read is modulated by the Floating Body effect.



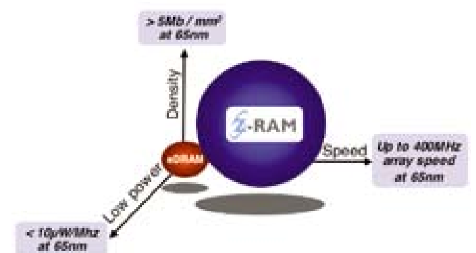


Figure 2. Z-RAM Performance Metrics

E2E

Ultra-Thin Body & Box (UTB²) SOI

By Thomas Skotnicki, Advanced Devices Program Director, STMicroelectronics, www.st.com

As we approach the end of the roadmap, single gate FD SOI devices with ultra-thin BOX could pre-empt the need for double gate devices.

It is well known that UTB (Ultra Thin Body) devices present improved electrostatic integrity. We were, however, among the first to report [1] on the importance of the BOX thickness with respect to the electrostatic integrity of SOI devices.

The electrostatics of FD SOI devices (we'll focus on DIBL — Drain Induced Barrier Lowering – a widely used figure of merit for MOSFETs) can be captured within the following simple equation [2]:

$$DIBL = 0.8\frac{\varepsilon_{si}}{\varepsilon_{ox}}\times\left(1+\frac{T_{si}^2}{L_{el}^2}\right)\times\frac{T_{ox}}{L_{el}}\frac{T_{si}+\gamma T_{box}}{L_{el}}\times V_{ds}$$

It confirms that with SOI, DIBL reduces not only with thinner top Silicon Film (Tsi), but also with thinner BOX.

How thin?

The practical question then arises: how thin should the BOX be? As shown in Figure 1, thinning the BOX from 150nm down to roughly 50nm is not very productive since the curve remains more or less flat. In contrast, beyond 40nm the curve drops down and the gain in DIBL is becoming significant.

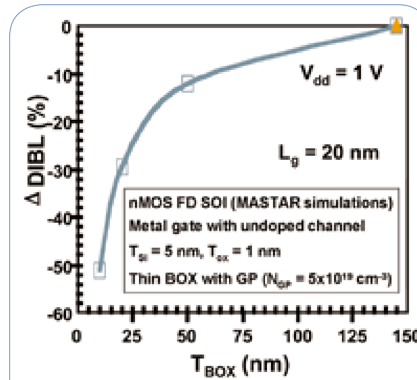


Figure 1. Reduction in DIBL as a function of BOX thickness (MASTAR simulations, [2]).

For the BOX thickness of 10nm, as much as a 50% reduction in DIBL can be expected. Beyond 10nm, as we have shown [3], the speed of the device starts to deteriorate due to an enhanced coupling with the substrate via the thin BOX. Therefore, 20nm BOX seems to be a good and secure compromise.

These practical requirements (20nm BOX) set a big challenge to SOI wafer makers, but also constitute an enormous opportunity for SOI technology.

The effect of BOX thickness is less than that of silicon thickness. Nevertheless, the use of ultra-thin BOX enables us to approach the electrostatics of Double Gate devices, while still remaining within the Single Gate scheme. CMOS integration on Ultra Thin Body & BOX SOI (we call it UTB²) may be technologically much simpler than any known Double Gate technology, and thus may be a battle horse for end-of-the-roadmap CMOS.

References:

1. T. Skotnicki et al., ECS 2003 Paris, ULSI Process Integration III pp.503-518 & SOI Technology and Devices XI pp. 133-148

2. T. Skotnicki et al., MASTAR Guide and Software via the metalink in the 2005 edition of ITRS (http://www.itrs.net/models.html)

3. T. Skotnicki, 2004 Symp. On VLSI Technology, Short Course Proceedings.

SOI Substrates with Ultra-Thin BOX

By Karine Landry, Project Manager, Advanced Technology Department, Soitec, www.soitec.com

Soitec is now sampling 25nm-thick UT-BOX.

Advanced SOI with ultra thin buried oxide (UT-BOX), in which the insulating BOX layer is less than 50nm thick, brings additional benefits to SOI CMOS architecture. It enables:

- electrostatic control of the device by back biasing, allowing ultra-low power operation through dynamic Vt control [1, 2].
- the definition of new memory device architectures such as capacitor-less one-transistor DRAM cells based on the floating body effect [2, 3].
- in combination with a FD MOSFET architecture, the potential elimination of the Vt fluctuation issue related to statistical dopant fluctuation (which at 45nm is cited as impacting SRAM stability).

To support the industry's evaluation of UT-BOX SOI, a Soitec R&D effort is developing 300mm SOI wafers with BOX thickness ranging from 50nm down to 10nm. As with all of Soitec's UNIBOND™ family of wafers, the UT-BOX SOI wafers are fabricated using Smart Cut™ technology.

UT-BOX development

In certain device architectures such as floating body memory cells or for back gate control, BOX plays an active role. In these cases, BOX characterization requires more specific attention both in terms of thickness uniformity and electrical oxide quality.

BOX uniformity of 1nm (on wafer min-max) has been attained. Buried oxide charge and buried interface quality are similar or better than mature SOI product. The breakdown field, which is a critical parameter for such thicknesses, is higher than 10MV.cm⁻¹, typical for gate oxides of such thicknesses.

Soitec's 25nm thick UT-BOX products currently under development will be commercially available in 2008, in time for the 45nm technology node. The defectivity monitoring curve in Figure 1 shows the learning curve with a typical defectivity at 0.15µm threshold lower than 0.15 def./cm². This quality allows us to sample R&D prototypes so that our partners can evaluate this technology both at the device and circuit level.

Customer feedback indicates that UT-BOX gives chipmakers additional "knobs" to further optimize device architecture and opens new areas of investigation.

In preparation for the 32nm node, early sampling of 10nm-thick UT-BOX is scheduled for the first half of 2007.

References

1- Fenouillet-Beranger et al., Solid-State Electronics 48 (2004)

2- Tsuchiya et al. IEDM 2004

3- Shino et al., IEDM 2004

4- Minami et al., IEDM 2005

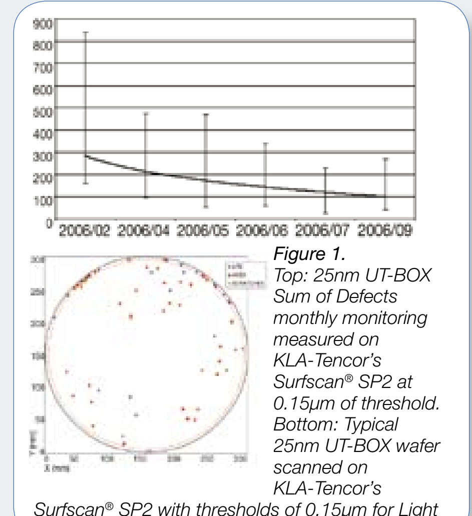


Figure 1. Top: 25nm UT-BOX Sum of Defects monthly monitoring measured on KLA-Tencor's Surfscan® SP2 at 0.15µm of threshold. Bottom: Typical 25nm UT-BOX wafer scanned on KLA-Tencor's Surfscan® SP2 with thresholds of 0.15µm for Light

R&D OUTLOOK

UT BOX SOI: Engineering for Future Low-Power Applications

By Carlos Mazure, CTO, Soitec, www.soitec.com

Ultra-thin buried oxide may solve some key design challenges at 32nm.

Leading-edge microprocessors built on SOI have maximized performance while respecting the power budget by decoupling the Si surface from the substrate with a 150nm-thick buried oxide (BOX).

However, moving towards low-power, high- or mid-performance CMOS applications, an increased coupling between the top layer of silicon and the handle substrate becomes paradoxically interesting. Reducing the BOX thickness provides several benefits.

For example, fully depleted (FD) IC architecture is highly suited for low power design, but is not compatible with a multi-threshold voltage (multi V_T) design. Taking advantage of a back gate bias through the substrate will set the V_T at different levels throughout the circuit without high dose implants, which are technically difficult for FD devices.

> Reducing the BOX thickness provides several benefits.

Furthermore, the designer will be able to work with the substrate doping without additional implants, thus maximizing carrier mobility, eliminating V_T mismatch due to dopant fluctuation in implanted channels and reducing short channel effects. All this while assuring the Ion/Ioff ratio > 10^6.

The BOX thickness required to assure sufficient back gate control at VDD<1V without the need for area-consuming charge pumps is in the range between 10 to 25nm. Thus ultra-thin BOX (UT-BOX) will have to guarantee an oxide integrity comparable to that of gate oxides.

At present the development of UT BOX SOI substrates is mainly driven by floating body cell DRAM and FD MOSFET applications. However, UT-BOX SOI CMOS constitutes a serious challenger for FinFET devices at the 32nm technology node.

PROFESSOR'S PERSPECTIVE

Nanomembranes: Just Around the Bend

By Max G. Lagally, E.W. Mueller Professor, Department of Materials Science and Engineering, University of Wisconsin-Madison, www.engr.wisc.edu

Starting with SOI wafers, Professor Lagally's team has developed strain-engineered silicon nanomembranes that could pave the way to flexible, high-speed circuits and more.

SOI, beyond its well-known use in CMOS devices, provides the foundation for a new class of structures: strain engineered Si nanomembranes. These membranes offer the promise for new devices or increased performance in applications as diverse as high-speed flexible electronics, light detection and imaging, piezoresistive devices, nanoelectromechanical-systems (NEMS) and other nanosensors, and potentially light emission.

Membranes offer flexibility, light weight, easy integration with many other materials, and possibly higher device densities. The strain offers higher CMOS device speeds and controllable modification of the band structure. These features enable new directions for the use of Si in electronics, photonics, and thermoelectrics, and the integration of Si with magnetic and ferroic materials.

> We expect that Si nanomembranes, based on SOI or variants of SOI, will form a technology platform that will enable many new semiconductor devices or improvements in current ones.

Why SOI?

The ability to etch the buried oxide in SOI selectively creates thin single-crystal sheets of silicon that are quite flexible and transferable to any number of other hosts. More importantly, by heteroepitaxial growth of Ge alloy on the SOI before oxide etching to release the membrane, uniform lattice strain can be introduced without the creation of dislocations.

Fast and flexible

A simple example of an elastically strained Si nanomembrane is a Si/SiGe/Si sandwich, in which the SiGe alloy strains the Si layers. Tensile strains of 0.4% are readily obtained in a 3-layer membrane that is 200nm thick. Such strains significantly raise the electron mobility.

All conventional Si processing is possible in such membranes. Because the membranes are flexible, transferable, and readily bondable to new hosts, they form the basis of very fast flexible electronics. Figure 1 shows thin-film transistors (TFTs) fabricated in a strained Si/SiGe/Si membrane and an image of a sheet of TFTs transferred to plastic. Because a Si/SiGe/Si membrane has two free Si surfaces, fabrication of devices on both sides is possible using simple membrane transfer processes.

Improved photodetectors

As a second example, Si nanomembranes may have a potentially high impact in photodetectors with improved speed or resolution. By integrating Si and Ge alloy nanomembranes in thin multilayer structures, we can fabricate PIN diodes, either on solid SOI or transferred to flexible substrates, in which the intrinsic layer is Ge or SiGe and the p-type and n-type layers are Si.

Membrane structures with higher degrees of complexity are possible, using known epitaxial growth techniques. Membranes can also be fabricated into various shapes using appropriate strain engineering. We expect that Si nanomembranes, based on SOI or variants of SOI, will form a technology platform that will enable many new semiconductor devices or improvements in current ones.

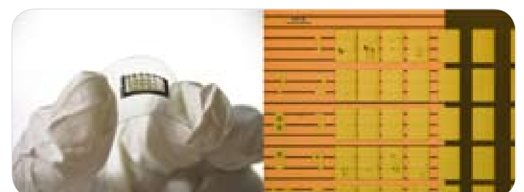


Figure 1. Thin-film transistors fabricated in a strained-Si nanomembrane and transferred to PET. (Courtesy: Haochih Yuan and The Lagally Research Group)

PEOPLE

Laurent Malier Named CEO of CEA-Leti

New leader for one of world's top microelectronics labs and original home of Smart Cut™ technology.

Dr. Laurent Malier has been named as the new CEO of CEA-Leti, one of the world's leading microelectronics laboratories. Dr. Malier, who holds a PhD in solid state physics, joined Leti two years ago from a major US company in photonic components.

Headquartered in Grenoble, France, Leti's activities cover micro- and nanoelectronics, microsystems and wafer-scale integration, devices for biology and health, wireless communications and imaging. It has one of the world's biggest and most advanced 200 and 300mm research facilities, enabling the research, development and testing of new materials, processes and devices in real conditions.

Dr. Laurent Malier
CEO, CEA-Leti

"Leti's added value in research stems from our cross-disciplinary approach and our model of collaboration with leading industrial and research organizations," says Malier.

Research activities are ongoing with eight major chipmakers and more than 50 suppliers. The lab has an annual budget of over 175 million Euros and a staff of over 1500. Of its 1200+ patents, more than 40% are licensed.

Leti has a strong tradition in advanced substrate innovation. For example, Soitec's Smart Cut™ technology was invented by Leti researcher Michel Bruel in the early 1990's. Leti and Soitec continue to pursue innovation and progress in advanced substrates through joint research teams.

For more information, go to www-leti.cea.fr.

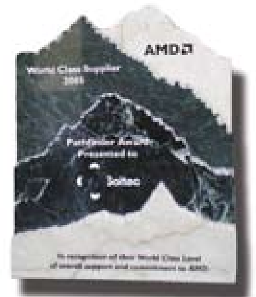
AMD Names Soitec as Best Wafer Fab Materials Supplier

World Class Supplier Pathfinder Award recognizes support and commitment.

AMD presented its annual *WCS Pathfinder Award for Best Wafer Fab Materials Supplier* to Soitec during a recent awards banquet in Dresden, Germany, home to AMD's Fab 30 and AMD Fab 36 manufacturing facilities.

"AMD's continued product innovation and customer success is closely linked to the suppliers we depend on for materials and support," said Alex Brown, vice president of global supply management for AMD. "We are pleased to recognize the outstanding support of our world class suppliers for their technical innovation, quality and high levels of service."

Soitec received the award in recognition of the company's world-class level of overall support and commitment to AMD in 2005. Soitec offers a comprehensive portfolio of engineered substrates including SOI and strained SOI based on its proprietary Smart Cut™ technology.



WCS Pathfinder Award for Best Wafer Fab Materials Supplier, 2005. (Courtesy: AMD)

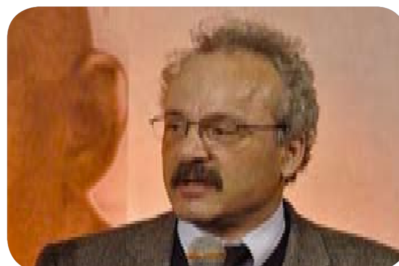
Simon Deleonibus Recognized as IEEE Fellow

Leti lab director and inventor of the principle of contact plugs now leveraging advanced substrates.

In further recognition of his distinguished career, Dr. Simon Deleonibus, Director of Leti's Electronic Nanodevices Laboratory, was recently awarded the grade of IEEE Fellow "for contributions to nanoscaled CMOS devices technology". This follows on other recent awards including the Grand Prize of the French Academy of Technologies and the Knight of the National Order of Merit by the French Presidency.

The author of over 300 papers and holder of 28 patents, he is well known as the inventor of the principle of contact plugs, now used in integrated circuits worldwide.

He and his Leti team leveraged SOI in 1999 when they set the world record for smallest transistor, with a 20nm gate length and 4nm channel length.

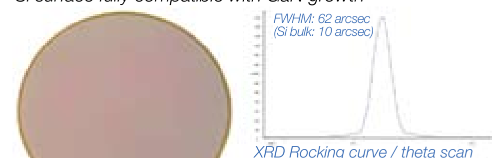


Dr. Simon Deleonibus, IEEE Fellow, receiving the "Grand Prix de l'Académie des Technologies – Prix Chéreau Lavet- 2005"

Today, he is an enthusiastic advocate of advanced substrates. "The great majority of our devices architectures from 65nm down to sub-22nm are achieved on SOI or other related engineered substrates," he says. "SOI gives you enormous flexibility in designing new devices architectures. Double-gate CMOS, FinFETs, FD and PD devices: we've pushed them down to sub-10nm gate lengths (5nm range channel lengths)."

SOI and other engineered substrates leveraging a wide range of materials and technologies, he speculates, may well be the Holy Grail in the eternal quest for low-power, high-performance applications.

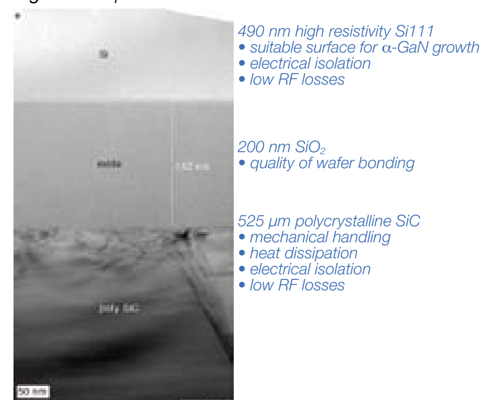
Figure 1. SopSiC surface
Si surface fully compatible with GaN growth



100 mm SopSiC substrate before GaN epitaxy

Top Silicon crystal quality not degraded and suitable to subsequent GaN epitaxial growth

Figure 2. SopSiC TEM



Surface (Fig.1) and TEM (Fig. 2) of a typical 100mm SopSiC substrate fabricated using Smart Cut™ technology. (Courtesy: Picogiga)

FROM THE FOUNDRY

Chartered's SOI Success Story

Chartered is the industry's first pure-play foundry to expand into high-volume SOI production.

By Dr. Liang-Choo "LC" Hsia, Senior Vice President, Technology Development, Chartered Semiconductor Manufacturing Ltd., www.charteredsemi.com

High-volume SOI at Chartered Semiconductor Manufacturing is a great success. January 2007 marks the three-year anniversary of the initial announcement that we would manufacture 90nm SOI products for IBM in volume-driven, high-performance solutions. Since we ramped production in mid-2005, we have shipped product on over 65K SOI wafers.

Yield has been excellent. In fact, since things like STI gapfill and CMP are easier, yield in SOI can be better than bulk if you know how to handle it.

New markets

Balancing power and performance are key requirements in a variety of products. To that end, Chartered and IBM have been collaborating closely with vendors to develop and validate SOI IP on the Common Platform. The Design Enablement Program ensures that design layout files can be used interchangeably across manufacturing facilities at our company and IBM.

> Yield in SOI can be better than bulk if you know how to handle it.

In April 2006, Chartered announced the licensing of IBM's 90nm SOI technology. That means we can offer SOI for consumer, multi-media, communications, automotive and industrial applications.

In parallel, Chartered has an active alliance program. We are expanding our collaboration with our value-chain partnerships to develop a comprehensive ecosystem of EDA tools, libraries and design IP in support of our SOI process technologies.

Although the barriers to SOI for the fabless world may seem high, we are well on our way to breaking them down.

Chartered's SOI Milestones

- **Q104 - First IBM SOI announcement**
  90nm SOI products for IBM in volume-driven, high-performance solutions beginning in mid-2005 (including Xbox™ 360).
- **Q404 - First AMD announcement**
  AMD64 microprocessors beginning in 2006.
- **Q205 - Start of volume SOI production in Fab 7**
  Integration of parts of **AMD's Automation Precision Manufacturing (APM)** helps attain world-class defect density.
- **Q405 - Microsoft starts shipping Xbox 360**
  First public demonstration of the IBM-Chartered Common Platform. Same GDSII database manufactured in high volume at two separate fabs half a world apart. Customer benefits: dual sourcing, single design, multi-sourcing with zero porting/re-design investment and much reduced risk.
- **Q206 - AMD starts revenue shipments of 90nm AMD64 CPUs manufactured by Chartered**
  Production ramped in record time, **hitting all major milestones and starting production at mature yields.**
- **Q206 - Licensing of 90nm SOI technology from IBM**
  Enables Chartered to expand SOI **to consumer, multi-media, communications, automotive and industrial applications.**
- **Q107 – Scheduled shipment of Microsoft Xbox 360 CPUs at 65nm**
- **Q207 – Scheduled transition to 65nm for AMD64 products**

III-V CORNER

Composite Substrates Promise Boost for GaN RF

Results of the HYPHEN project indicate a new path to high-volume, high-power, and high-frequency wireless applications.

By Philippe Bove, Picogiga R&D Director, www.picogiga.com and HYPHEN Project Leader, www.hyphen-eu.com

The European HYPHEN GaN-RF project is developing and evaluating new types of composite substrates based on silicon and silicon carbide materials. These new substrates are designed to provide cost-efficient solutions for advanced high-power devices used in wireless communication systems such as radar, satellite communications and base stations.

During the first year of this three-year project, we compared the industry's two standard materials – GaN on bulk silicon and GaN on bulk SiC – with GaN grown on two of the most promising composite, engineered substrates: silicon on poly-crystalline silicon carbide (SopSiC); and SiC on poly-crystalline SiC (SiCopSiC). These substrates were engineered using Soitec's Smart Cut™ technology.

More reliable epitaxy

The initial material characterization results show that all the critical performance factors (crystal quality, mobility, surface morphology and so forth) of GaN on composite substrate materials are equal to or even better than the current industry standard materials. These substrate comparisons were assessed using the two most established epitaxy techniques: metallic organic CVD (MOCVD) and molecular beam epitaxy (MBE).

> Preliminary results show the epitaxy of GaN HEMT on SopSiC composite substrates is more reliable than on conventional silicon substrates. It is also substantially cheaper and better suited to high volumes than bulk SiC substrates.

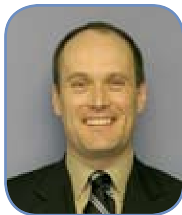
The new composite substrates also demonstrated superior results in terms of pilot production yield and repeatability. According to the preliminary results, the epitaxy of GaN HEMT on SopSiC composite substrates is more reliable than on conventional silicon substrates. SopSiC as a substrate for GaN growth also has the advantage of being substantially cheaper and better suited to high-volumes than bulk SiC substrates.

The HYPHEN project is developing and characterizing the complete technology chain, from substrate to GaN HEMT device. The second phase, which is now underway, involves device processing.

Project partners include: Picogiga, University of Padova DEI, Alcatel-Thales III-V Lab, the Research Institute for Technical Physics and Material Science (Hungary), Norstel, Institute of Electron Technology (Poland), IEMN/CNRS (France) and UMS. The work is partially supported by the European Community, under the Innovation Society Technologies (IST) program of the 6th Framework Program.

MEMS

Micragem™ – An SOI-based MEMS Process Platform



By Bruce Alton, Vice President, Marketing & Business Development, Micralyne, www.micralyne.com

Micralyne's robust, standardized fabrication process reduces time-to-market.

One key issue companies face is time-to-market — how long it takes to move a MEMS-based product from an idea to generating revenues. Micragem™ is an SOI-based MEMS fabrication process with a set of design and process guidelines used to prototype and manufacture different types of MEMS components in a standardized fashion. Developing a product based on Micragem™ reduces time-to-market by taking advantage of Micralyne's existing characterized processes.

SOI technology was originally developed to avoid charge leakage in p-n junctions, but due to the robustness of the single crystal device layer as a structural material for silicon microstructures, SOI substrates are also attractive to MEMS applications. Micralyne developed Micragem™ as a prototyping process on SOI that is simple, versatile, and mature.

The steps

At the basic level, Micragem™ is a four-mask lithography and wafer-bonding process:

- Mask 1: Thick glass wafer is patterned for the first etch.
- Mask 2: Metal is patterned on the glass substrate, both on the non-etched surface and in the etched features.
- Mask 3: Device layer of an SOI wafer is bonded to the glass wafer. The handle and BOX layers of the SOI are then removed. Micralyne's proprietary low stress gold is deposited on the silicon surface, and lithographically patterned to produce wires, bond pads, and reflective surfaces.
- Mask 4: The final process in the DRIE (Deep Reactive Ion Etch) to vertically etch the silicon patterns and release mechanical elements.

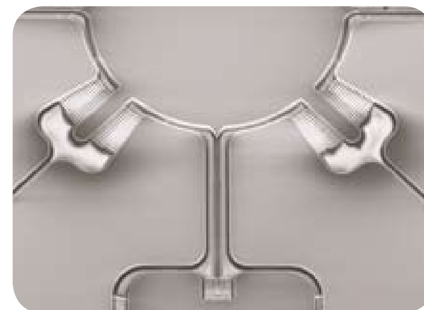
The result is a reliable, robust, and manufacturable MEMS device.

Faster, better, cheaper

The potential of this simple process platform in the MEMS field is substantial. The process is well suited to prototype miniaturized micro-mirrors, diaphragms, micro-channels, cantilever beams, valves, comb drives and much more. In turn, these devices can be used as the basis to produce products such as mirror-based optical switches that increase the speed of fiber optic networks, inertial devices for automotive safety applications, and pressure sensors that can accurately perform while withstanding extreme harsh environments.

The result is a reliable, robust, and manufacturable MEMS device.

Users of Micragem™ benefit by reducing MEMS development costs, creating higher levels of reliability and performance earlier in development, and efficiently prototyping and testing their new product ideas.



A MEMS optical switch mirror developed using the Micragem fabrication process. (Courtesy: Micralyne)

SHOPTALK

High-Speed Wafer Bonder Boosts SOI MEMS Productivity

By eliminating the need for heating and cooling, MHI's new system brings volume production to standard and SOI MEMS.

One of the advantages cited in SOI MEMS design is the ability to create more complex structures serving a wider range of applications. However, the industry's standard wafer-level packaging can be a challenge, as it typically needs to heat up the bonding materials, which takes time and can impact yield. To help bring SOI and other MEMS applications further into the mainstream, manufacturing systems are needed that enable high-speed, high-yield and low-cost processes.

In response, Mitsubishi Heavy Industries (MHI) has developed high-speed wafer-bonding equipment for MEMS applications. The system, which operates in a vacuum chamber, avoids thermal treatment by using ion-beam activation at the molecular level of the wafer surface. Benefits include:

- Elimination of thermal stress induced in the device, since it is a room temperature process;
- High throughput of vacuum-sealed devices, as there is no need for heating and/or cooling; and
- The choice of a broader selection of materials, including: silicon, silicon dioxide, oxides (including some ceramics), compound materials, metals and hetero materials.

This enables a very high degree of accuracy and miniaturization in vacuum-sealed devices. Three-wafer bonding is also available for the future hybrid MEMS devices.

The MHI high-speed wafer bonder for MEMS is distributed by the Seika Corporation.
More information can be obtained from soi@jp.seika.com.

MHI's high-speed wafer-bonder increases packaging throughput for SOI and standard MEMS applications. (Courtesy: Mitsubishi Heavy Industries)

GUEST SPOT

SOI Wafer Market Outlook: Enjoying Firm Growth, While Looking for New Applications

By Takashi Ogawa, Research Vice President, Dataquest Semiconductors, www.gartner.com

Gartner Dataquest sees the potential for market expansion and "bold decisions".

Gartner Dataquest has been conducting research on the SOI wafer market trend since 1995. Its results indicate that SOI wafer demand achieved a compound annual growth rate (CAGR) of 33% over the decade between 1995 and 2005.

In particular, the principal thin film segment enjoys strong growth recently due to the burgeoning consumer electronics demand, including video games, as well as a major drive from data processing applications. Likewise, the thick film segment also experiences healthy growth partly because of successful exploration of new applications such as PDP drivers and automotive applications.

> The most likely scenario forecast indicates that SOI wafer demand will achieve a CAGR of 31% between 2005 and 2010.

Driving adopters

While leading-edge device vendors, such as IBM and AMD, firmly maintain their position as early adopters of SOI technology, the short-term outlook suggests that the activities of these companies will drive the SOI market, even if a major event does not occur.

On the other hand, for the SOI wafer market to enter a fully-fledged stage in the medium and long run (after 2008), adoption by vendors with volume consumption (so-called "early majority") is essential as the second wave of propagation following the early adopters. While early adopters are ready to accept any obstacle — regardless of its extent or scale — and work with it to find a solution, because they have established their dominance in the market, early majority vendors with volume consumption are reluctant to introduce a new technology unless its advantage or prospect becomes visibly clear.

In fact, this constitutes a chasm between the two groups of vendors. Filling such a chasm to encourage technology adoption by early majority vendors requires further technology innovation, such as significant cost reduction, and a clear move for market formation to help establish a competitive advantage in a particular domain. Gartner Dataquest has made the scenario forecast based on the wave of vendors' movement.

Innovation wild card

Figure 1 shows SOI wafer demand forecast under each scenario. Under the most likely scenario, SOI wafer demand will be driven by early adopters in 2006 and 2007, with the annual growth rate exceeding 40% each. In 2008 and afterwards, it will go over the peak and the growth rate will enter the downtrend. The most likely scenario forecast indicates that SOI wafer demand will achieve a CAGR of 31% between 2005 and 2010, totaling 243.7 MSIs in 2010, including captive demand.

A key point in estimating the market outlook is, unlike ordinary market forecast, the fact that "innovation" that can achieve a breakthrough in the market expansion process will likely play an important role, while it is difficult to forecast the emergence of such innovation accurately.

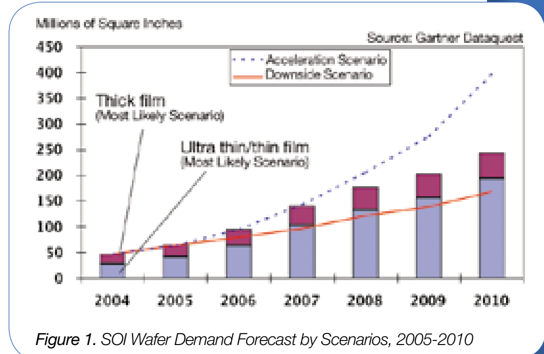


Figure 1. SOI Wafer Demand Forecast by Scenarios, 2005-2010

In particular, in expansion of leading-edge technology markets such as SOI wafer, the supply of key leading-edge technology and the creation of innovation by the "lead user" can achieve a (unexpected) breakthrough, as proposed by Professor E. V. Hippel of MIT Sloan School of Management, which can then often lead to market expansion. In this context, SOI technology can be considered to have significant market potential.

Bold attitudes

Also, for successful commercialization of new technology or market expansion, other factors than technology issues, such as creating product planning and marketing, also play a critical role. To promote the development of a breakthrough technology or significant market expansion, bold decisions and endeavors under proper risk management is essential and care should be taken not to fall into a myopic conservatism. The development of SOI technology and business, which continue since 1995, is said to be the outcome of "bold decisions and endeavors" mostly led by European and American semiconductor vendors. It is expected that such bold attitudes will become pervasive among Japanese and Asia/Pacific counterparts.

PAPERLINKS HIGHLIGHT

STM *et al* Win IEEE '06 SOI Conference Best Paper

RF on thin HR SOI can open the door to low-cost, mass-market 200GHz applications in the coming year.

A paper presented by STMicroelectronics in conjunction with IMEP UMR and IEMN, entitled "State of the art 200 GHz passive components and circuits integrated in advanced thin SOI CMOS technology on High Resistivity substrate" (F. Gianesello *et al*) won Best Paper Award at the IEEE 2006 SOI Conference.

The paper concluded that HR SOI can be used in the coming year to open up the V, W and G bands (up to at least 200GHz) – previously the domain of expensive III-V technologies – to low-cost, mass-market CMOS digital and RF/MMW applications.

For the full PAPERLINKS and CALENDAR listings, featuring top papers from recent conferences as well as links to upcoming events, see www.advancedsubstratenews.com.

EDITORIAL

Strong and Stronger

By Adele Hars, Editor-In-Chief

The SOI ecosystem is growing.

At a recent Soitec-sponsored conference of industry leaders — some committed to SOI, some still thinking about it — the high energy level and increasing enthusiasm for advanced substrate technology was clear as the mountain air.

We heard top OEMs talk about what they needed in a chip, and top chipmakers, designers and suppliers talk about what they were doing to meet those needs. Listening to each other, it was clear that an SOI ecosystem is well underway.

With the news that ARM – the chip industry's leading IP provider – is joining in, we have clear confirmation that SOI is moving into the vast realm of high-growth, consumer-driven applications.

Today's watchwords are power, price and performance. SOI is the keystone.

▸ Two new SOI-based chips from **IBM**: the PowerPC 750CL consumes half the energy of its predecessor and runs at 400MHz to 1GHz; the PowerPC 970GX, a follow-on to the PowerPC 970FX, maintains the power level but incorporates twice the integrated L2 cache.

▸ **IBM**'s SOI-based **Cell** processor news:

- IBM's first Cell-Based BladeCenter Systems, targeting the aerospace, oil & gas and medical industries, are shipping.
- **Mercury** Computer Systems, which is shipping Cell-based systems to customers in medical imaging, industrial inspection, supercomputing, semiconductor design and manufacturing, and defense-industry signal processing, is reporting **performance gains of greater than an order of magnitude** in performance/inch^3, /pound, /Watt or /dollar. It also announced the first Cell Accelerator Board for PCs.
- Dubbed "Roadrunner", the supercomputer going into the DOE's Los Alamos Labs has over 16,000 AMD Opteron™ processor cores and over 16,000 Cell B.E. processors. Peak performance: **over 1.6 petaflops** (1.6 thousand trillion calculations/second).

▸ **AMD** (which builds all their 64-bit microprocessors on SOI) news:

- Having acquired ATI, AMD plans a new class of "Fusion" processors **integrating the CPU/GPU at the silicon level**. Scheduled for 2008/ 2009 delivery, the chips will target laptops, desktops, workstations, servers, consumer electronics and emerging markets.
- The native Quad-Core Opteron processor, (four cores on a single silicon die) has taped out and will ship in mid-2007.

▸ **Freescale** is rolling out **application-specific additions to its 85xx, SOI-based PowerQUICC III communications processors**: the MPC8568E and MPC8567E with a Gigahertz CPU core for multi-protocol interworking in broadband access equipment (samples Q107); the MPC8572 for application-aware content processing at multi-Gigabit speeds in networking and communications equipment; and the MPC8533E, an SoC optimized for fanless operation and low power-consumption in high-speed, hard-copy office equipment.

▸ **Atmel** is using SOI instead of bulk BCDMOS for it SMARTIS™ technology. Result: chips in its new driver-IC family for automotive high-temperature applications are more reliable and can run at up to 200°C (150°C ambient). That means they can go very close to a hot engine to control flaps in turbochargers or exhaust gas recirculation systems. Likewise, for the ATA6826 driver IC for controlling body electronics (the industry's first automotive load driver IC on SOI), SOI simplifies manufacturing and enables a reduction in chip size. Result: improved EMC performance and maximum reliability at less than $1/chip.

News Flash

ARM Moves Into SOI

ARM Holdings, the industry's leading provider of semiconductor **IP for processors, peripherals and SoC solutions**, is strengthening its physical IP portfolio by adding SOI technology.

Buys SOISIC

"SOI technology is a leading candidate to address the power and performance scaling issues associated with traditional bulk CMOS processes as they migrate to ever-smaller geometries. The acquisition of SOISIC adds a new capability to our physical IP portfolio, offering the potential for significantly better optimization of performance and power consumption for our Partners."

— Mike Muller, CTO & Director, ARM

Partners with Soitec

"We are extremely pleased to see ARM supporting the SOI ecosystem. We look forward to partnering with them to further develop the design infrastructure that will be critical to the high-performance, low-power consumption chips that SOI enables."

— André-Jacques Auberton-Hervé, President and CEO, Soitec

▸ **Luxtera** announced new technology that multiplexes four 10Gbps wavelengths onto a single fiber, on a production SOI CMOS die – resulting in a single fiber 40Gbps link. This reduces cost and paves the technological way **for 100Gbps Ethernet** data center connectivity. Earlier, the company sampled the first monolithic devices containing combined lasers and SOI CMOS photonic circuits in a commercially feasible transceiver configuration. The technologies will be used in a commercial transceiver product line launching in 2007.

▸ **Toshiba** America Electronic Components announced an SOI-based family of high-voltage, three-phase motor drivers for DC motors and inverters used in home appliances and industrial products. SOI helps enable higher power with lower power consumption, faster response time, and higher levels of integration, all in a small structure.

▸ **Frost & Sullivan** has a new report on "Emerging Trends in SOI Technology". It includes key drivers, challenges, restraints, analysis and forecasts of the technologies it says may shape the future of the semiconductor industry.

▸ **Intel** announced a hybrid silicon laser, which consists of an InP laser cavity that is directly bonded to a waveguide formed in an SOI substrate. Large numbers of such light emitters can be placed in one monolithic structure and provide very high bandwidth communication between microprocessor chips or even between individual cores.

▸ Construction is underway of **Soitec**'s new 300-mm SOI wafer fab in Singapore. Dubbed Pasir Ris 1, it will start supplying customers in mid-2008, as it ramps to a final production capacity of one million wafers per year. The Group is also expanding its production capacity in France.

Thank you!

A special thanks goes to our colleagues at Sony, IBM, Nintendo, Microsoft, DFC Intelligence, Hitachi, Winwatch, BCC Research, RFID Journal, Toshiba, Innovative Silicon, STMicroelectronics, Gartner/Dataquest, CEA/Leti, AMD, Chartered, Micralyne, MHI, U.Wisconsin-Madison, Soitec and Picogiga for their help with this issue.

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Please send your news and views to editorial@advancedsubstratenews.com.

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