

Thin-Layer Au-Sn Solder Bonding Process for Wafer-Level Packaging, Electrical Interconnections and MEMS Applications

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Abstract

The developed bonding process utilizes AuSn solder and provides liquid-proof sealing and multiple reliable electrical connections between the bonded wafers. The bond can withstand 300°C and features a thin bond line (2-3 μm), high bond strength, excellent bond gap control, and low stress due to small amount of bonding material. A Nb/Au seed layer was shown to be an optimal adhesion and barrier film.

Keywords:

Wafer bonding, AuSn solder, electrical interconnects, bond gap control, sealing, thin bond line, low stress bonding, adhesion layer, solder wetting.

Introduction

The results described in this paper were obtained within a development program for a MEMS-based memory device. Wafer-to-wafer bonding is a key process in wafer-level packaging (WLP). It can be used for both mechanical connection and electrical interconnections between wafers. However, there are no widely available industry-standard processes for wafer bonding particularly with precisely controlled small gaps between wafers. This work demonstrates a near-hermetic low-temperature and low-stress wafer bonding process with well-controlled bond gap of 2-3 μm.

Development Goals

The goal was to develop a wafer-to-wafer bonding process combining reliable electrical connections in multiple areas (~10³ per wafer), wafer-to-wafer separation of 2-3 μm, excellent bond gap control, high bond strength and a minimum of liquid-proof sealing. Liquid-proof sealing should allow further processing of the bonded stack – lithography, etching, etc. Besides these main requirements, the bonding process should not create large stresses (due to the bonding process itself and due to mismatch of the thermal expansion characteristics of materials) in the wafer stack, which would limit unwanted change in MEMS device performance due to stress relaxation. Preferably, the same process can be used for bonding of a third wafer to the stack of two bonded wafers.

Selection of Solder for Bonding Development

As Au-Au thermo-compression bond is unlikely to meet the sealing requirements and provide reliable electrical connections, solder bonding was considered as the main path. Potential candidates among solder bonding processes include AuSn, AuIn, CuSn, and AlGe bonding [1]. AuSn bonding, having an acceptable process temperature of about 300°C, has been used in many WLP applications [2] and therefore was chosen as a

basis for the development. However there are two disadvantages to the process: (a) typical thickness of the solder is 5-8 μm – much thicker than the target bond layer thickness and (b) the layer formed as a result of AuSn bonding is hard, thus creating built-in stress in the wafer stack.

AuIn allows bonding at 180°C [3-4] and the bond layer is much softer than that of AuSn. However, the process seems to be more challenging due to the very fast Au-In interdiffusion. It is less understood and is not widely accepted by industry.

AlGe system is known to provide good sealing, but the process requires temperatures above 400°C [5].

CuSn bonding was considered as an attractive candidate. However, published information is almost exclusively focused on multi-chip stacking and through silicon via technology. Using this process for WLP may reveal some difficulties.

Wafers for Bonding Tests

Two types of wafers were used in bonding development tests: “MEMS” wafers and “Cap” wafers or Caps. MEMS wafers represented functional wafers with MEMS structures while Caps were mechanical wafers. Cap wafers had standoffs defining final bond gap, plated Au-Sn solder and patterned seed layer. MEMS wafers had a patterned Au layer with the layout corresponding to that on the Cap wafers.

Fabrication of the Cap wafers is schematically shown in Fig. 1. Standard thickness 6” wafers with TTV smaller than 5 μm were used. After initial oxidation (A), standoffs were defined by oxide patterning. Caps re-oxidation followed (B). Typically, initial oxide thickness was close to 3.1 μm and 1.0 μm thick oxide was grown at the second oxidation step. Resulting height of the standoffs was close to 2.6 μm. Seed metal (4000 Å Au) was deposited on the Caps (C) and Au-Sn solder was plated using a photoresist mask (D) in the next steps. Initial plating tests were made using an R&D setup while later work was done using industrial-grade Cup plater from EEJA. Plated solder was 2.0-2.5 μm thick with 5-10% non-uniformity across wafer and contained about 65% of Au and 35% of Sn. Patterning of the seed metal layer was the last step in the pre-processing of Caps (E). The seed layer was left around the plated areas.

For bond development both silicon and glass substrates were used in place of actual MEMS wafers. Au was deposited and patterned on glass substrates before bonding. Silicon wafers went through initial oxidation followed by deposition and patterning of Au. Thickness of Au deposited on MEMS wafers was typically close to 4000 Å.

Each die had a 500 μm wide bond ring. The wafers also had a 7 mm exclusion zone (6 mm for the industrial plater) and a 1.5 mm wide wafer-level bond ring outside the exclusion zone. All bond rings were defined by patterning of the seed metal.

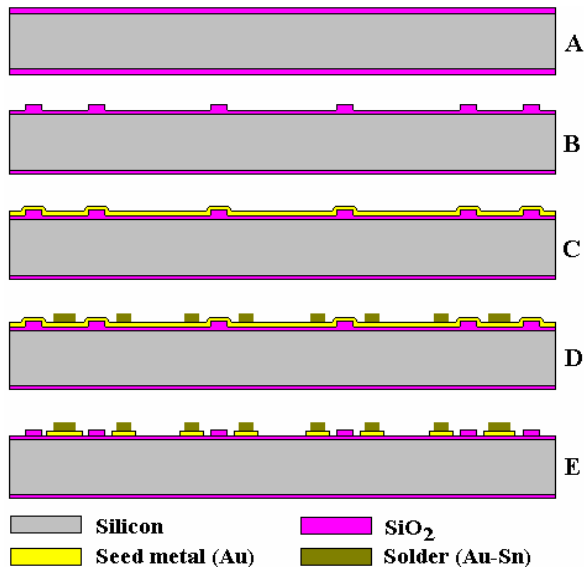


Fig. 1. Fabrication of Cap wafers for bonding tests

Different designs of the solder pattern were used (see Fig. 2), including single 280 μm wide ring (a), single ring with tabs (b-d) two 200 μm wide rings, three 60 μm wide rings (e-f) and five 36 μm wide rings. The interconnection areas had 80 μm x 100 μm rectangular seed areas with 60 μm x 80 μm plated Au-Sn posts. As a result of bonding, multiple sealed chambers surrounded by bond rings were formed. Pressure inside the chamber depends on the parameters of the bonding process.

Experimental Results

SB6e bonder (Suss) was used for wafer bonding. Most of the tests were done in vacuum. Maximum process temperature was 300 $^{\circ}\text{C}$ in most tests (320-350 $^{\circ}\text{C}$ in some tests). After bonding, wafer stacks were diced and inspected for delamination or damage. Silicon-glass stacks were also inspected for presence of water in the sealed chambers. The gap between wafers was measured on silicon-glass stacks using a Zygo profilometer. Initial bonding tests were made using wafers with TiW adhesion layer on both wafers. It was found that after melting solder can be easily compressed, but tends to flow out of seed metal areas causing unacceptable “spills” (see Fig. 3). Analysis of the samples showed that all Au was consumed in the areas where the solder was plated and most of the solder moved out of these areas (see Fig. 4) due to poor wetting of TiW by Au-Sn. Although bond strength was good, solder re-distribution sometimes caused flooding of cavities at dicing and, in some cases, even die delamination was observed.

Several alternative adhesion layers were tested to address the TiW/AuSn de-wetting issues. The TiW/NiV adhesion layer with TiW completely covered by NiV did not exhibit dewetting. However, limited flow and poor compression of solder was observed in the presence of Ni. Analysis of the bonding metal stack showed that solder-seed interface is tin-depleted (see Fig. 5). Most likely this was caused by Ni-Sn interaction, forming an alloy. Loss of tin increases melting temperature of Au-Sn alloy, so that the solder does not melt in at least some areas. Moreover, on several wafers with TiW/NiV adhesion film, the gap measured after bonding was actually larger than expected based on the thickness of all bonding layers. Increasing dwell time at high temperature did not help in solder flow, but reduced bond strength possibly due to loss of adhesion. Reducing amount of Ni in the system by decreasing

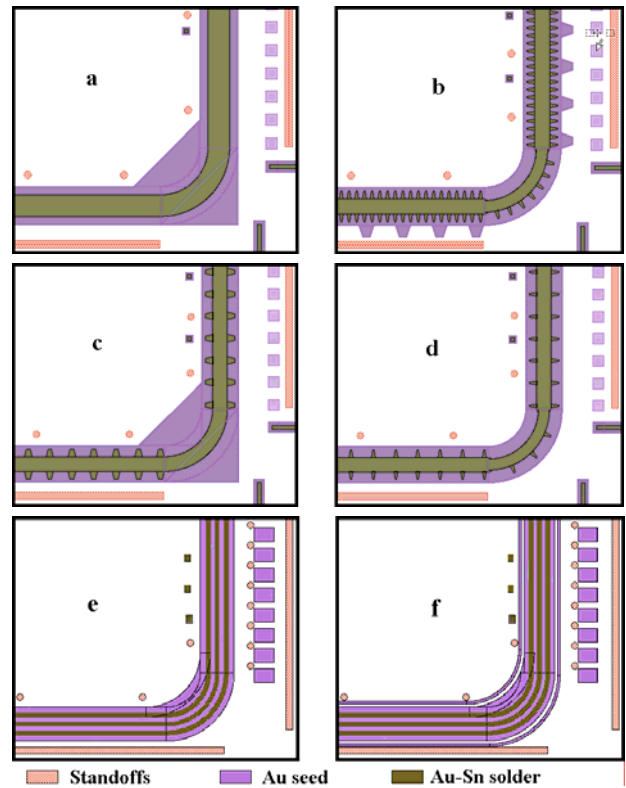


Fig.2. Solder patterns used in wafer bonding development

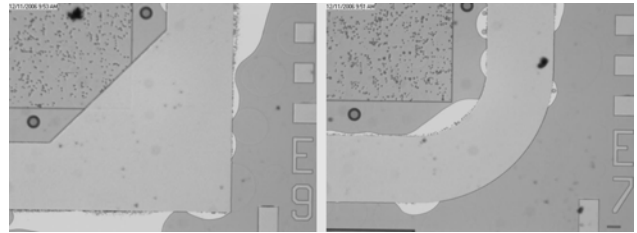


Fig. 3. Solder “spills” after bonding wafers with TiW adhesion layer. Pictures are taken through glass substrate.

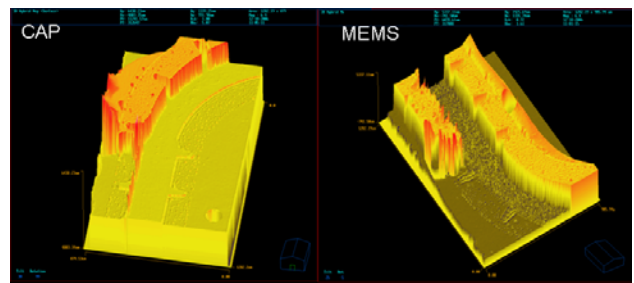


Fig. 4. Solder distribution after bonding with TiW adhesion layer measured by optical profilometer on open sample. Most of solder moved out of the area where it was plated.

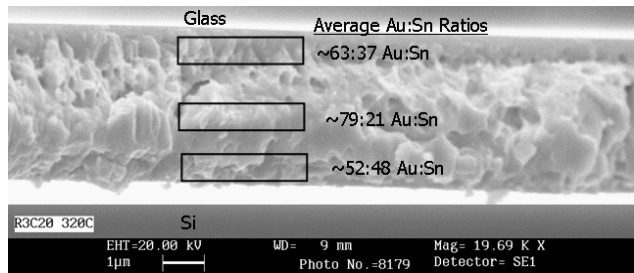


Fig. 5. Au-Sn composition measured in different areas of the bond layer cross-section

thickness of NiV in TiW/NiV stack to 150 Å did not improve solder flow. Bond strength was good, but the required bond gap control could not be provided with TiW/NiV adhesion layer.

Both Ti/Au and Ti/Mo/Au metallization allowed solder flow and provided for a very strong bond. However, solder de-wetting similar to TiW/Au metallization was observed and as a result sealing of cavities was not liquid-proof.

Metallization with adhesion layers containing Cr (Cr/Au and NiCr/Au) was found to lose adhesion at the interface with SiO₂ after bonding. Good solder compression was observed in the case of a Cr adhesion layer. However, almost no solder compression was found in the case of NiCr adhesion layer.

The best results were obtained using Nb adhesion layer [6]. Good solder wetting, solder flow, exceptionally strong bond, good sealing of cavities as well as full transfer of electrical lines from one wafer to another were obtained. The wafer-to-wafer gap for the developed process is close to 2.6 µm, as determined by the height of the standoffs.

When a bonded chip was opened, it never separated at solder interfaces, but usually broke leaving either Si or glass in the bonded areas. After bonding in vacuum, Newton rings were typically observed in all areas corresponding to sealed cavities indicating that they are still under vacuum. Processing of the wafer stacks bonded with Nb/Au seed layer showed that the seal is liquid proof. Use of Nb seed layer allowed to reduce the amount of solder needed for wafer bonding, decreasing plating area to less than 4% of wafer surface and resulting in significant reduction of thermo-mechanical component of stress in the wafer stack.

Another aspect of the development was related to evaluation of different solder patterns. It was found that designs with narrow (50-60 µm) solder lines exhibit better flow and provide better sealing than designs with wide solder lines.

Design Considerations for Bonding Pattern

Au-Sn composition close to eutectic (80% Au : 20% Sn) needs to be formed during bonding for solder flow. Deviation from the eutectic composition results in significant increase of the melting temperature for the Au-Sn alloy. Au-Sn phase diagram shows that eutectic temperature is 278°C; alloys with 81% (wt) and 75% (wt) of Au melt at 340°C and 333°C, correspondingly. Fig. 6 is a diagram of bonding stack before and after bonding. Experimental data shows that a thin Au seed layer (4000 Å) contacting the solder can be all consumed during bonding. Moreover, as liquefied solder is squeezed during bonding, some additional Au is consumed in the seed areas flooded with melted solder. Gold diffusion into the solder is fast. Au concentration at the periphery of the bond ring can be higher than in the center due to diffusion of the additional Au. Within wide solder lines Au concentration can be lower in the center and higher at the periphery making squeezing of the solder difficult. For this reason, narrow solder lines can be preferable. Assuming that final gap is determined by height H of standoffs, the amount of Au and Sn in the bond ring can be evaluated based on density ρ_s, thickness T_s and width L_{solder} of the plated AuSn layer, concentration of Au and Sn (C_{Au} and C_{Sn}) in the solder, thickness of the seed and adhesion layer (T_{Au} and T_{adh}).

All tin comes from solder. Its amount per unit length is equal to:

$$B_{Sn} = \rho_s \cdot L_{solder} \cdot T_s \cdot C_{Sn} \quad (1)$$

Both the solder and the seed layer are sources of Au. Maximum amount of Au that can be transferred to the bond ring in case of full consumption of seed layer with a width of L_{bond}, as it is shown in Fig. 6, is equal to:

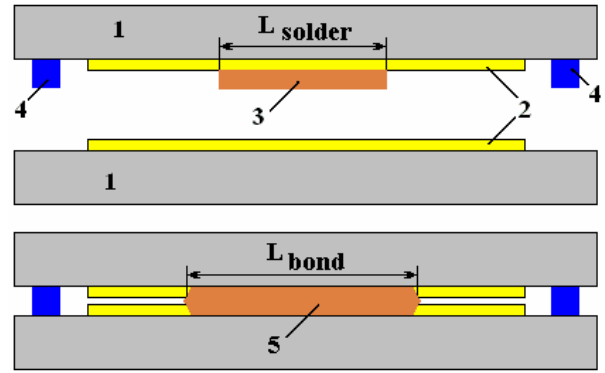


Fig. 6. Geometry of plated solder and bonded area. 1 – substrates for bonding; 2 – Au seed layer; 3 – plated Au-Sn solder; 4 – standoffs; 5 – bond ring formed as a result of bonding.

$$B_{Au} = \rho_s \cdot L_{solder} \cdot T_s \cdot C_{Au} + 2 \cdot \rho_{Au} \cdot L_{bond} \cdot T_{Au} \quad (2)$$

Final width of bond ring L_{bond} can be found by equating mass of materials per unit length before and after bonding as follows:

$$\rho_s \cdot L_{solder} \cdot T_s + 2 \cdot \rho_{Au} \cdot L_{bond} \cdot T_{Au} = \rho_s \cdot L_{bond} \cdot (H - 2 \cdot T_{adh}) \quad (3)$$

Width of the bond ring L_{bond} can be evaluated from (3).

Ratio of B_{Au} to B_{Sn} defined by (1) and (2) allows for evaluation of Au-Sn alloy composition forming the bond ring. Varying either the thickness and/or composition of plated solder or thickness of Au seed layer can change the composition. It is safer for target Au concentration in Au-Sn alloy to be slightly lower than 80%, allowing for process variation.

Conclusion

Effect of adhesion layer is more important when 2-3 µm thick layers of metal are used for Au-Sn wafer/die solder bonding than in the case of traditionally used 5-8 µm thick bonding layers because of two reasons. First, all Au from the seed layer can diffuse into the melt and wetting of adhesion layer by Au-Sn solder can affect the bond. Second, fast diffusion of metals in thin seed layer can introduce intermetallics that can affect solder melting and/or flow, in particular, by affecting concentration of Sn. Adhesion layers containing Ni or Nb give strong bonds. However, solder has limited flow in the presence of Ni. Adhesion layers containing Ti and Mo exhibit poor solder wetting. Films containing Cr can lose adhesion after bonding. It is important to account for Au available within bonding area taking into account compression of the solder during bonding.

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