MicraGEM-Si™

A flexible process platform for complex MEMS devices

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Introduction

MicraGEM-Si™ is a process platform for MEMS prototyping and research offered by Micralyne Inc. This technology is a silicon-on-insulator (SOI) based MEMS process for academic and industrial users to develop devices such as micro mirrors, optical switches, resonators, inertial and bio sensors.

The technology offers:

- Two thick SOI structure layers with up to three functional levels of silicon thickness on the Base device layer.
- The Top device layer has a silicon etch in the back side as well as a release etch from the top side.
- Deep etch features in the Base and the release etch in the Top device layer are aligned to better than 0.4 µm. This capability enables structures like vertical comb drive actuators.
- Base and Top device layers are electrically connected through the bond interface, allowing 3D routing of electrical signals.
- Patterned low-stress gold metallization on the top surface is suited for highly reflective mirrors and contact pads for gold wire bonding.

Micralyne has partnered with CMC Microsystems to make this process available to companies and researchers as part of a Multi-Product Wafer program. This allows customers to purchase a portion of a MEMS fabrication run based on a 4 mm x 4 mm die size. Upon completion of the fabrication run, each client will receive a quantity of individual or packaged die. Larger die sizes are available by request (4 x 8 mm, 8 x 8 mm). CMC Microsystems provides the front end sales, delivery of the design kit, including a design rule checker, and the consolidation of designs for Micralyne to build.

For design kit details and ordering visit:
https://www.cmc.ca/MicraGEM-Si

MicraGEM-Si™ Platform Description

The process platform includes a powerful combination of established MEMS technologies. The Engineering team at Micralyne has leveraged its extensive experience in developing bulk machined MEMS devices to create a standard platform designed to enable a wide variety of MEMS structures. Key processes within the platform include high aspect ratio Deep Reactive Ion Etch (DRIE), aligned wafer to wafer bonding, non-contact stepper photolithography, and low stress mirror metallization.

Stepper lithography provides non-contact exposures with excellent repeatability, consistency, alignment accuracy, throughput, and quality. Micralyne has demonstrated that silicon fingers in a precisely aligned staggered pattern can be maintained when using 3D wafer stacking. With thoughtful process design, out-of-plane features can be aligned to within 0.4 µm overlay tolerance.

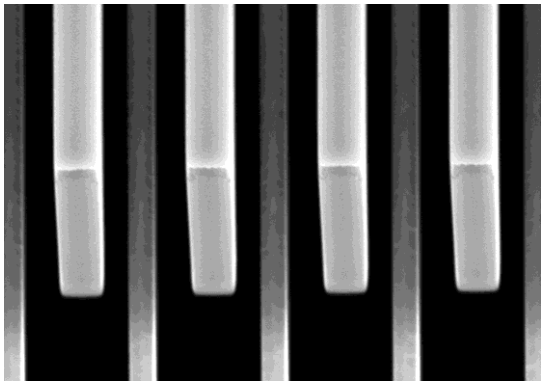


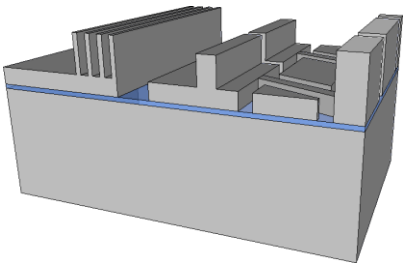
Figure 1: Vertical comb drive actuator

This process flow can used to create a vertical comb drive actuator, which is an important structure in the fabrication of advanced optical MEMS **(Figure 1)**. The comb drive actuator provides nearly linear tilt response to the applied voltage at high angles. A well designed comb drive actuator can also significantly reduce the voltage requirement to achieve maximum tilt.

MIcraGEM-Si™ Fabrication Flow

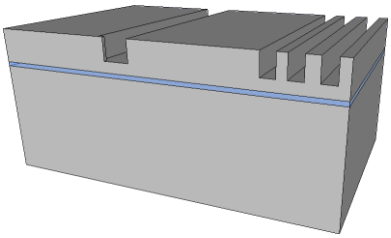
Step 1: Define Trench 1, Trench 2 and Trench 3 on Base Wafer

The device layer thickness of the Base wafer is 50 µm. The regions defined as Trench 1 are etched to a final depth of 50 µm (all the way through the device layer). Trench 2 regions are etched to a final depth of 35 µm, leaving a 15 µm high section of silicon sitting on the buried oxide of the Base SOI. Trench 3 regions are etched to a final depth of 10 µm, leaving a silicon region with a height of 40 µm sitting on the Base SOI. With these three regions, many complex 3D silicon structures can be created including cavities, electrodes and wires for electrical routing, as well as lower combs for vertical comb drive actuators.



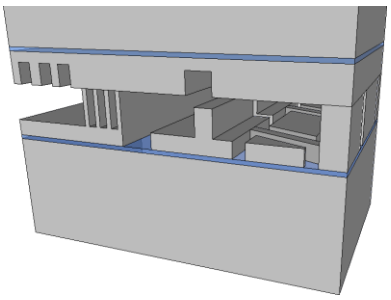
Step 2: Define and Etch Top SOI Wafer Backside

The Top SOI wafer is patterned and etched to a depth of 20 µm. Once the Top SOI wafer is bonded and the handle wafer is removed, this will leave a suspended region of silicon with a 10 µm thickness.



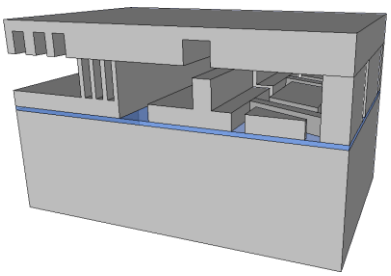
Step 3: Bond Base Wafer to Top Wafer

Once the Base Wafer and Top wafer have completed the DRIE etch processes, the wafers are aligned and fusion bonded in a controlled environment. The accuracy of the wafer alignment after the completed fusion bond is +/-10 µm.



Step 4: Remove Top SOI Handle and Buried Oxide

After fusion bond, the handle of the Top wafer is removed with a grind and polish process. The buried oxide of the Top wafer is also removed leaving a pristine optically flat silicon surface.



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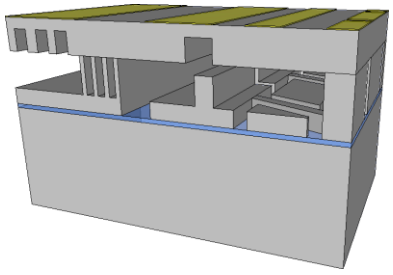
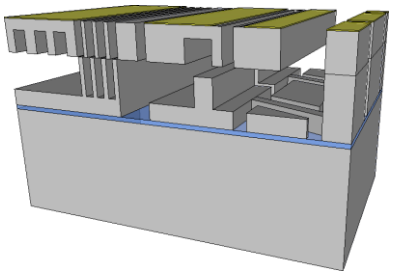
Step 5: Deposit and Define Metal

The Top device layer is blanket coated with a low stress TiW/Au metallization. This is then patterned to form device elements such as electrodes, bond pads, and highly reflective surfaces.



Step 6: Release Pattern and Etching

The final DRIE process etches completely through the Top device layer and releases the MEMS structures.

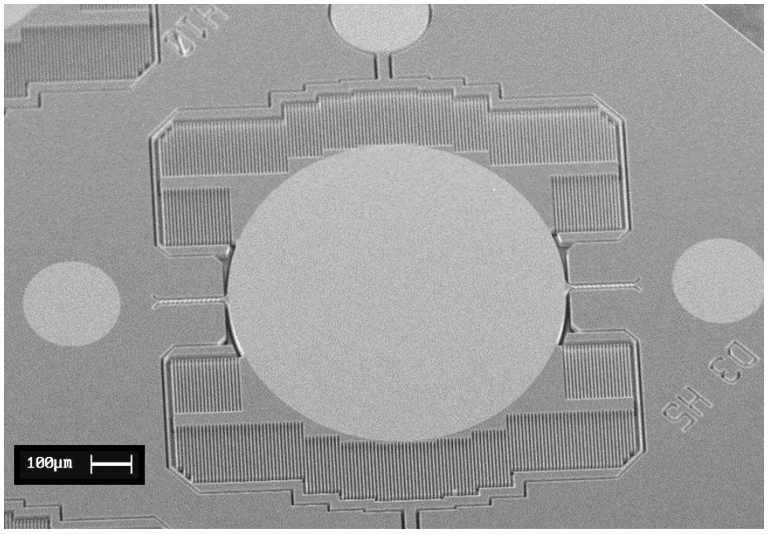


Step 7: Singulation

The dicing process is done with a laser which enables singulation without damaging the released MEMS devices.

Figure 2:
MicraGEM-Si Process

Example – Variable Optical Attenuator (VOA) MEMS Chip



The MicraGEM-Si™ platform is ideal for fabricating simple uni-directional (1D) tilting optical devices **(Figure 3)**. These can be configured for use in variable optical attenuators (VOA) and low port count wavelength selective switch (WSS) modules. With the MicraGEM-Si™ platform you can create arrays of mirrors driven by vertical comb drives. The result is an array of mirrors requiring low actuation voltage and linear voltage-theta curve within its designed operating range **(Figure 4)**.

Figure 3: SEM Micrograph of the VOA Chip – demo device

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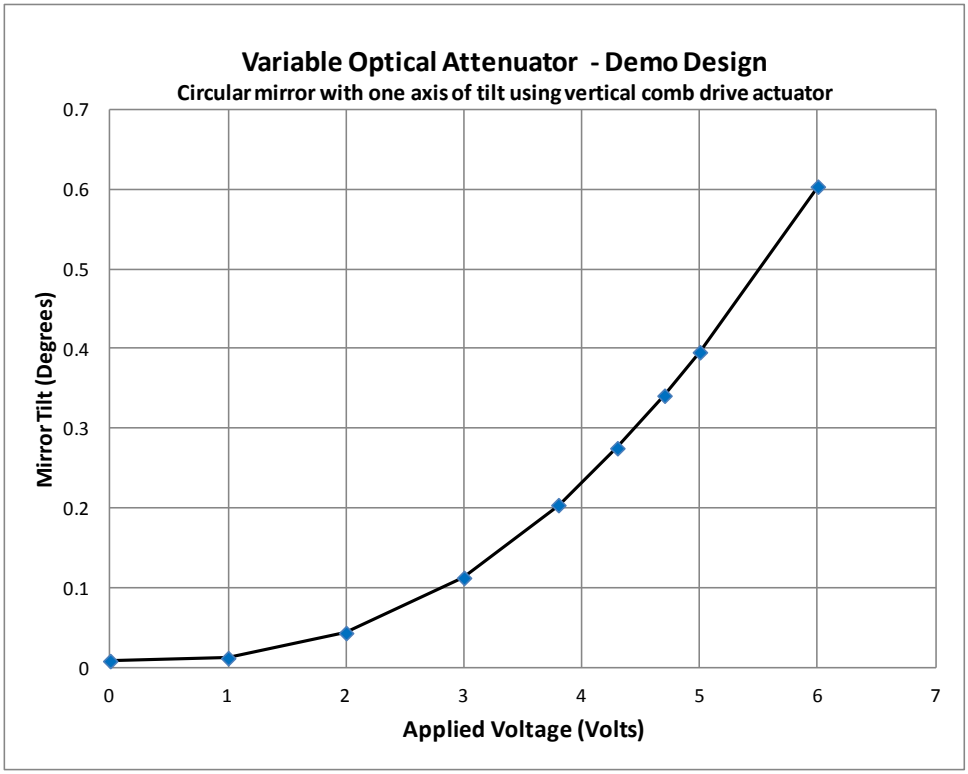
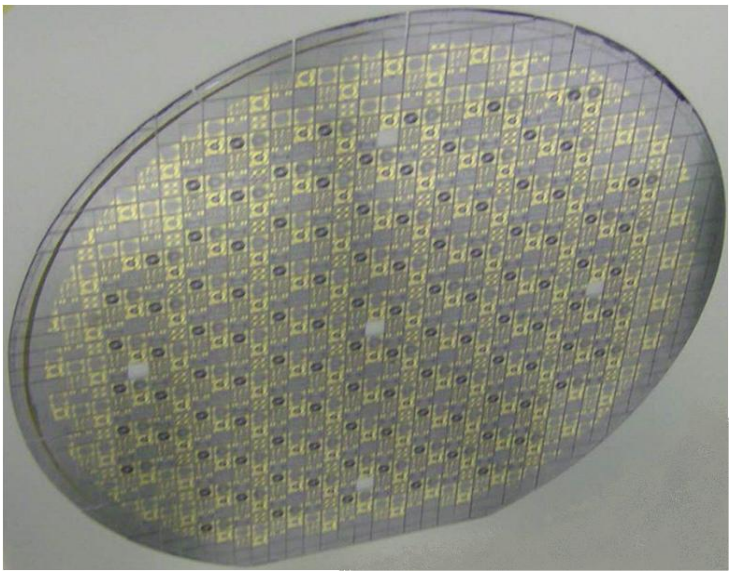


Figure 4: MEMS for VOA - Mirror tilt response to an applied voltage

The demonstration MEMS chip was designed to meet specific parameters for low voltage. Theoretically, a 1 mm diameter mirror can have a tilt of up to 4 degrees if voltage is not constrained. This platform is suitable for deflection of a mirror flat towards the Base wafer. Horizontal comb drives can also be created for use in inertial sensors. The creativity of the designers will also provide unlimited possibilities for structures, devices, and applications.

Summary

Micralyne has presented a process platform that provides the benefits of a vertical comb drive and other key MEMS structures, in an elegant and highly manufacturable format. Devices designed with MicraGEM-Si™ will be able to quickly ramp in to volume production.



MicraGEM-Si™ Wafer